IN THE SPECIFICATION:

Please make correction to paragraphs 15 and 17, as marked.

[0015] By creating design practices that avoid cache and memory coherency issues, the processor can be placed into a low power state. When the memory space used by the driver is marked and maintained as non-cacheable, memory coherency issues go away. Marking this memory space as non-cacheable assures that copies of this memory space are not present in the processor's cache and that there is no need to snoop the processor's cache for any bus master accesses by the device that uses this memory area. When the BM_STS is designed to [NOT] not be set when a device generates bus master operations to the non-cacheable memory space, the BM_STS bit will not be set during these memory operations and the OS can place the processor into the low power C3 state more often.

[0017] To optimize the entry of the C3 state, the following table illustrates how the BM_STS should be set depending on the cache ability of the memory area being accessed:

Type of Bus Master Cycle	Current BM_STS	Improved BM_STS
Memory Read Non-Cacheable Memory	Set	[No change] Not Set
Memory Write Non-Cacheable Memory	Set	[No change] Not Set
Memory Read Write-through Cacheable Memory	Set	[No change] Not Set
Memory Write Write-through Cacheable Memory	Set	Set

Type of Bus Master Cycle	Current BM_STS	Improved BM_STS
Memory Read Write-back Cacheable Memory	Set	Set
Memory Write Write-back Cacheable Memory	Set	Set

As the table shows, making the bus master buffers non-cacheable totally avoids setting the BM_STS bit, while making bus master buffers write-through cacheable avoids setting the BM_STS bit for any read cycles. Depending on the behavior of the bus master, one of these techniques may be applied to allow the processor to enter into the C3 state more often.